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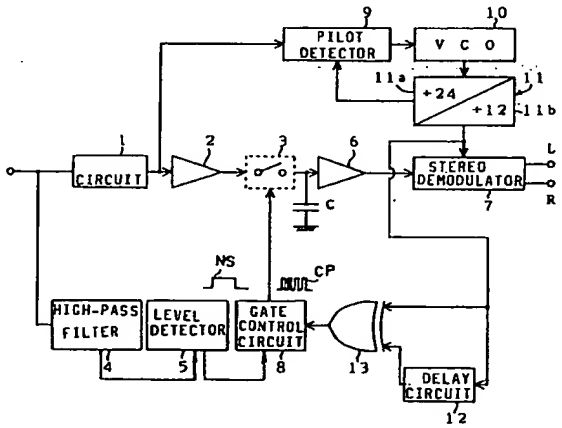
(54) Noise suppressing circuit in an FM tuner.

(57) A noise suppressing circuit has a gate for controlling a composite signal applied to a stereo demodulator of an FM tuner, and a detector for detecting a noise included in the composite signal and for producing a noise dependent signal for controlling the gate to close it. A pilot signal detector is provided for detecting a pilot signal included in the composite signal for producing a pilot dependent pulses. In response to the noise dependent signal and to the pilot dependent pulses, gate control pulses are applied to the gate, thereby closing the gate in synchronism with the pilot signal.

FIG. 1



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BACKGROUND OF THE INVENTION

The present invention relates to a noise suppressing circuit for suppressing pulse noises and multipath noises in an FM tuner.

In order to avoid radio disturbance in the FM tuner caused by various noises such as pulse noises and multipath noises, there are provided various systems in the FM tuners.

Fig. 3 shows a conventional noise suppressing circuit. A composite signal obtained through a front end, an intermediate frequency amplifier and a detector (not shown) of the FM tuner is applied to a delay circuit 1 for delaying the signal. The delayed signal is applied to a gate 3 through a buffer amplifier 2. On the other hand, the composite signal is applied to a level detector 5 through a high-pass filter 4. The level detector 5 detects noises to produce output signals for closing the gate 3. The composite signal passes through the opened gate 3 and is charged in a capacitor C.

Fig. 4 shows the voltage at the capacitor C. If the noises N are included in the composite signal, the gate 3 is closed, so that the capacitor C holds the voltage during a period T corresponding to the overlapping period of the noise N as shown in Figs. 5a and 5b. Thus, the composite signal is cut off for the period T.

The composite signal from the gate 3 is applied to a stereo demodulator 7 through a buffer amplifier 6. The composite signal is demodulated by the stereo demodulator 7 based on a pilot signal to provide an audio signal having right (R) and left (L) signals.

Thus, noises are eliminated, so that sound having good sound quality if obtained.

However, if the closing time of the gate 3 becomes long, a sub signal included in the composite signal is reduced, which causes the demodulated signal to distort. In the conventional circuit, therefore, the closing time of the gate 3 is set to 10 μsec to 20 μsec by a timer provided in a gate control circuit (not shown). However, the noise can not be completely eliminated.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a noise suppressing circuit which may reliably eliminate various noises.

According to the present invention, there is provided a noise suppressing circuit in a FM tuner having a gate for controlling a composite signal applied to a stereo demodulator of the FM tuner, a capacitor for charging a voltage at an output terminal of the gate, and a detector for detecting a noise included in the composite signal and for producing a noise dependent signal for controlling the gate to close it.

The circuit comprises a pilot signal detector for detecting pilot signal included in the composite signal and for producing a pilot dependent pulses, gate control circuit means responsive to the noise dependent signal and to the pilot dependent pulses for producing gate control pulses in synchronism with the pilot signal, the gate being responsive to each of the gate control pluses to be closes.

In an aspect of the invention, the gate control circuit means includes an exclusive OR gate responsive to the pilot dependent pulses, and a gate control circuit responsive to the noise dependent signal and to output pulses of the exclusive OR gate for producing the gate control pulses by dividing the noise dependent signal with the output pulses.

The other object and features of this invention will become understood from the following description with reference to the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 shows noise suppressing circuit according to the present invention;
Fig. 2a shows a waveform of a gate control signal from a gate control circuit of the circuit;
Fig. 2b shows a waveform of a composite signal controlled a gate of the circuit;
Fig. 3 is a conventional noise suppressing circuit;
Fig. 4 shows a waveform of a composite signal including noises in the conventional circuit;
Fig. 5a shows a time chart of a gate of the conventional circuit; and
Fig. 5b shows a waveform of a composite signal controlled by a gate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 1, a noise suppressing circuit of the present invention has the same elements as the conventional noise eliminating circuit of Fig. 3 as delay circuit 1, buffer amplifier 2, gate 3, high-pass filter 4, level detector 5, capacitor C, buffer amplifier 6, and stereo demodulator 7.

The circuit further comprises a gate control circuit 8 connected between the level detector 5 and the gate 3. The delay circuit 1 is further connected to a pilot detector 9 for detecting a pilot signal included in the composite signal. The pilot detector 9 is connected to a voltage-controlled oscillator (VCO) 10 which is connected to a frequency divider 11 having a 1/24 divider 11a and a 1/12 divider 11b. The 1/24 divider 11a is connected to the pilot detector 9. The 1/12 divider 11b is connected to the stereo demodulator 7, a delay circuit

12 and an exclusive OR gate 13. The output of the delay circuit 12 is connected to the exclusive OR gate 13 which is in turn connected to the gate control circuit 8.

Describing the operation, the delayed composite signal from the delay circuit 1 is applied to the buffer amplifier 2 and the pilot detector 9. The pilot detector 9 detects the pilot signal in the composite signal and produces a pilot base signal which is applied to the VCO 10. The VCO starts oscillation based on the pilot base signal voltage of the input signal. An oscillated signal is applied to the frequency divider 11. A signal having a frequency divided in the 1/24 divider 11a is fed back to the pilot detector 9. A signal having frequency divided in the 1/12 divider 11b is applied to the demodulator 7, delay circuit 12 and an input terminal of the exclusive OR gate 13. In the delay circuit 12, the signal from the divider 11b is delayed, and a delayed signal is applied to the other input terminal of the exclusive OR gate 13. The exclusive OR gate 13 produces control pluses in accordance with the delayed signal and the signal without delaying which are applied to the gate control circuit 8.

On the other hand, the level detector 7 produces a noise dependent signal NS in accordance with noises included in the composite signal.

The gate control circuit 8 divides the signal NS into a plurality of gate control pulses CP each having a small pulse width in accordance with the input signal from the exclusive OR gate 13. The gate control pulses CP are applied to the gate 3 to close it. Therefore, the voltage at the output terminal of the gate 3 is held in the capacitor C at every control pulse CP.

Thus, the waveform of the output signal of the buffer amplifier 2 is approximately kept as shown in Fig. 2b. The demodulator 7 demodulates the composite signal from the buffer amplifier 6 to the audio signal based on the output from the 1/12 divider 11b. Thus, the sub signal in the composite signal is maintained so that sound having good sound quality is obtained.

In accordance with the present invention, the gate is controlled in synchronism with the pilot signal included in the composite signal. Thus, the sub signal included in the composite signal is prevented from reducing. Accordingly, it is possible to increase the opening time of the gate, thereby sufficiently suppressing the noises.

While the presently preferred embodiment of the present invention has been shown and described, it is to be understood that this disclosure is for the purpose of illustration and that various changes and modifications may be made without departing from the scope of the invention as set forth in the appended claims.

Claims

1. A noise suppressing circuit in an FM tuner having a gate for controlling a composite signal applied to a stereo demodulator of the FM tuner, a capacitor for charging a voltage at an output terminal of the gate, and a detector for detecting a noise included in the composite signal and for producing a noise dependent signal for controlling the gate to close it, the circuit comprising:

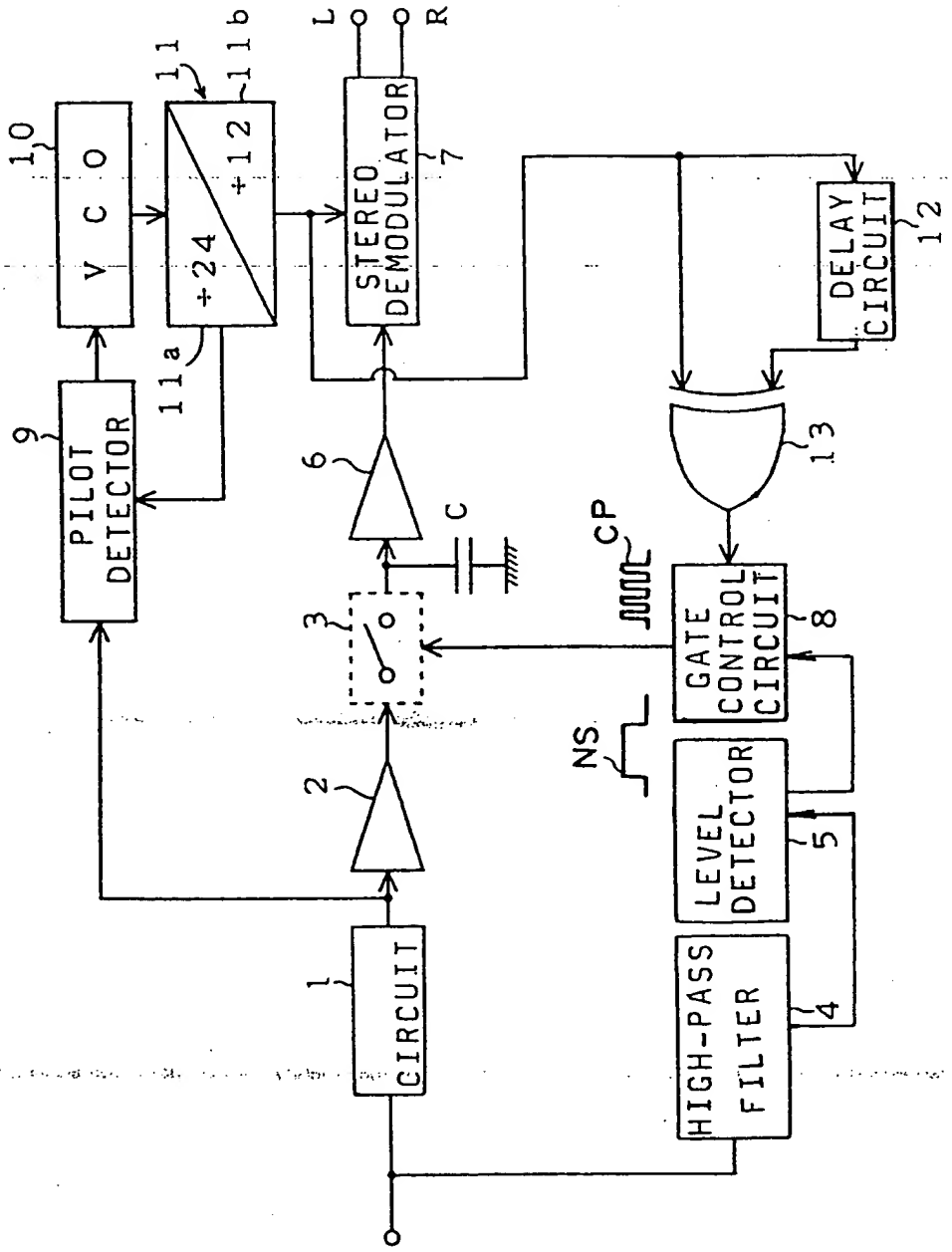
   a pilot signal detector for detecting a pilot signal included in the composite signal and for producing a pilot dependent pulses;

   gate control circuit means responsive to the noise dependent signal and to the pilot dependent pulses for producing gate control pulses in synchronism with the pilot signal,

   said gate being responsive to each of the gate control pulses to be closed.

2. The circuit according to claim 1 wherein the gate control circuit means includes an exclusive OR gate responsive to the pilot dependent pulses, and a gate control circuit responsive to the noise dependent signal and to output pulses of the exclusive OR gate for producing the gate control pulses by dividing the noise dependent signal with the output pulses.

FIG. 1


L
R
VCO
10
÷24
÷12
11
11a
11b
STEREO DEMODULATOR
7
DELAY CIRCUIT
12
PILOT DETECTOR
9
6
C
CP
13
3
GATE CONTROL CIRCUIT
8
NS
LEVEL DETECTOR
5
2
HIGH-PASS FILTER
4
1
CIRCUIT

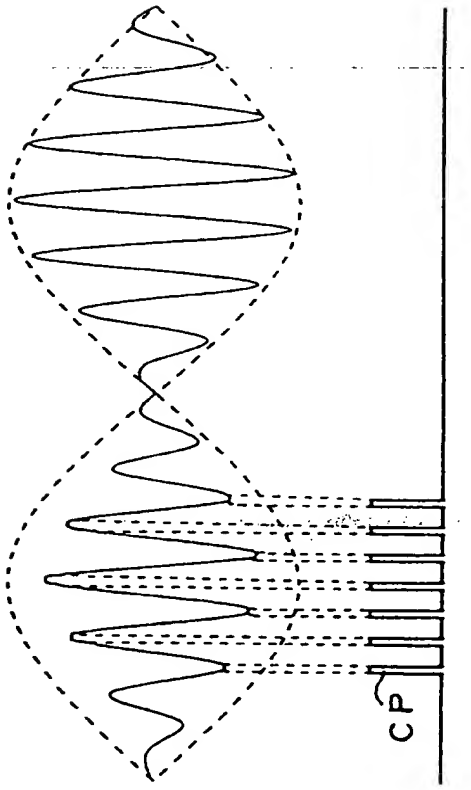


FIG. 2b

FIG. 2a

FIG. 3

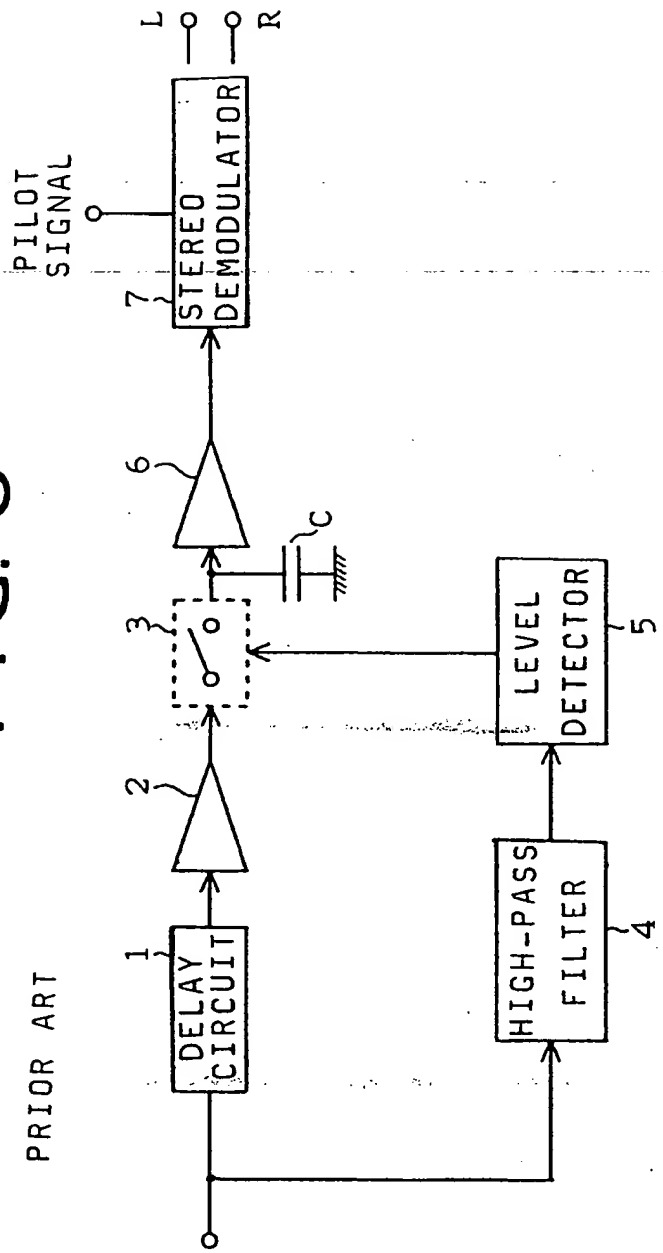
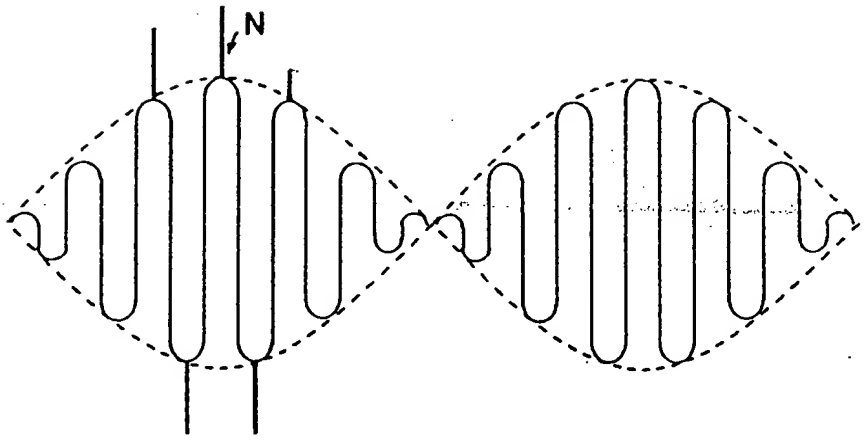

PRIOR ART
DELAY CIRCUIT
1
2
3
HIGH-PASS FILTER
4
LEVEL DETECTOR
5
6
C
7
STEREO DEMODULATOR
PILOT SIGNAL
L
R

FIG. 4

PRIOR ART



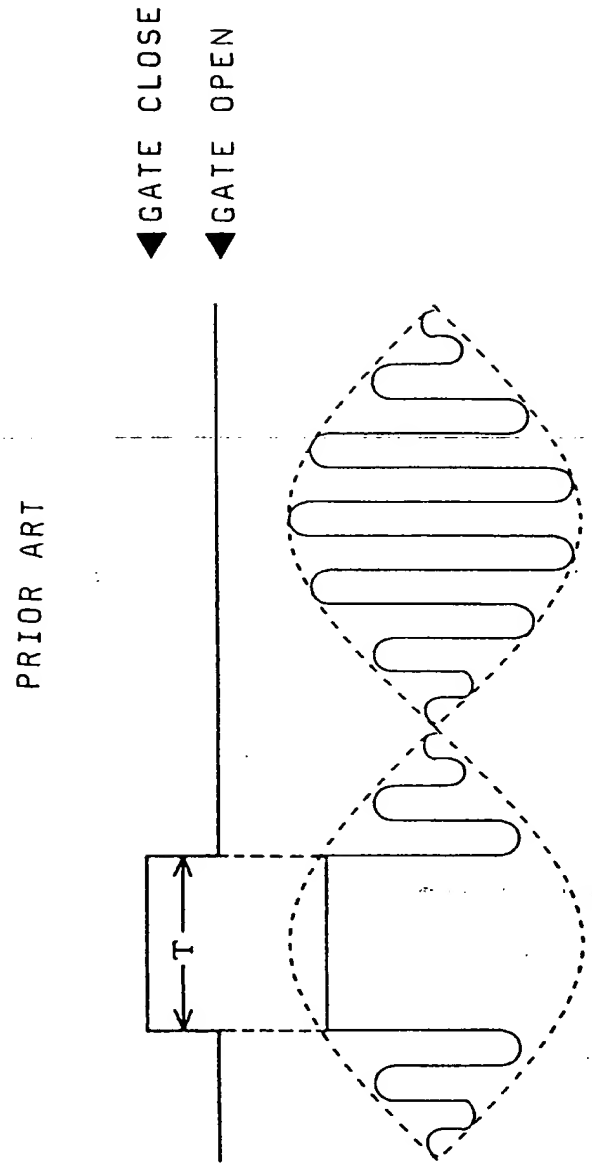


FIG. 5a

FIG. 5b